REMARKS/ARGUMENTS

A Final Office action was issued on February 2, 2010 in relation to the above referenced application. In the Final Office action, claims 1-6 are rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Pat. Publ. No. 2001/0018759 to Andreev et al. ("Andreev") in view of U.S. Pat. No. 5,742,510 to Rostoker et al. ("Rostoker").

Claims 1, 3, and 4 are pending. Claim 1 has been amended. Support for the amendment to claim 1 can be found in the application as filed. Applicant submits that no new matter has been added. Reconsideration and reexamination are respectfully requested. The Examiner is thanked for attention to the application.

It is noted that the Office action continues to assert that present claim 1 is obvious in view of Andreev when considered in combination with Rostoker. It is respectfully submitted that in fact claim 1 is not obvious, and in particular one of ordinary skill in the art would not have been capable of applying the technique of Rostoker to the method of Andreev. Furthermore, it is submitted that even if such a combination were capable of being applied, then the invention as presently claimed would still not result.

Before proceeding, Applicant suggests that a brief appraisal of the teachings of both Andreev and Rostoker is appropriate.

Andreev

Andreev relates to a method for routing nets in an integrated circuit design. To do this, account is taken of the connections to be made. As has been previously set out, and as Applicant believes that the Examiner accepts, Andreev does not route all connections independently and in parallel, as is specifically required by present claim 1. Instead, if two connections are overlapping (i.e. direct routing of each connection would cross) then Andreev works in the wholly conventional manner as follows:

i) one of the connections is routed initially,
ii) the routed connection is "locked down",
iii) the other connection is then routed.

In fact, this method is analogous to the prior art described in the present application. Since, with this method, the routing will depend on which connection is considered first, the method cannot be independent. In addition, since each connection is considered in turn, the method cannot be parallel. Accordingly, Andreev does not teach, "routing all connections of the printed circuit board electrical circuit independently and in parallel, wherein each connection is routed while ignoring all other connections", among other limitations recited in claim 1.

Rostoker

Rostoker is actually a rather different type of disclosure. It is submitted that while Rostoker attempts to claim wide ranging applications, even suggesting (col. 13 lines 58-64) that some of its techniques may be used for "financial market analysis" and "weather forecasting", Rostoker is predominantly aimed at solving "problems" (however disparate they may be) by assigning them to parallel processors (see e.g. col. 13, lines 47-50), rather than considering all specific tasks independently. In order to do so, a "problem" is decomposed into a number of processes that can be performed in parallel (see col. 21, lines 14-51), and performing them in parallel using the parallel processors.

In fact, it is submitted that Rostoker relates mainly to channel routing of integrated circuit chips, which is not suitable for printed circuit boards (PCBs), as will be discussed later.

In any case, Rostoker does not teach routing all required connections independently and in parallel as recited in claim 1. Take the following very simplified example, showing an initial problem where the A ports need to be connected, the B ports need to be connected, the C ports need to be connected, the D ports need to be connected:

B

A A

B

C

D D

C

It is immediately apparent that there is conflict between A and B, and between C and D, but no conflict between A and D for example.

Therefore, Rostoker determines that the problem can be broken down into two separate tasks or groups, one being the conflict between A and B, and the other being the conflict between C and D. According to Rostoker, each one of these tasks / groups is assigned to a processor, and these two tasks are worked on in parallel. This is clearly set out in Rostoker, see for example col. 16 lines 9-10, or col. 23, lines 18-26, or col. 26 lines 32-42.

However, it can also be seen that within each group, the solution will be wholly dependent on which connection is considered first. For example, taking the first group above comprising the A-A, B-B conflict, does the process route between A and A and then force B to connect along a longer path, or does the process route B-B first and then force A-A to take a longer path?

In other words, even though the problem as a whole has been "decomposed" (using the wording of Rostoker) into two separate processes, within each process the routing of each connection will still be performed serially, and thus not independently as required by the present invention. Accordingly, Rostoker does not teach, "routing all connections of the printed circuit board electrical circuit independently and in parallel, wherein each connection is routed while ignoring all other connections", among other limitations recited in claim 1.

Combining Andreev and Rostoker

Claim 1, as amended, recites, "routing all connections of the printed circuit board electrical circuit independently and in parallel, wherein each connection is routed while ignoring all other connections", among other limitations. For the reasons recited above, it is firstly noted that neither Andreev nor Rostoker disclose a method in which all required connections are routed in parallel and independently. Therefore, however Rostoker and Andreev are combined, there is no possibility of resulting in the present invention. For this reason alone, claim 1 must be patentable over Andreev and Rostoker.

Secondly, the proposed modification cannot render the prior art unsatisfactory for its intended purpose. (MPEP §2143.01). Andreev requires that in the case of a crossing conflict, a first connection is locked down, while other connections are considered. As indicated above, Rostoker is predominantly aimed at solving "problems" by assigning them to parallel processors (see e.g. col. 13, lines 47-50), rather than considering all specific tasks independently. By attempting to parallelize the serial process for handling crossing conflicts, it appears that the proposed modification would render Andreev unsatisfactory for its intended purpose. (MPEP §2143.01). For at least this reason, the proposed combination is improper, and claim 1 is patentable over the cited references.

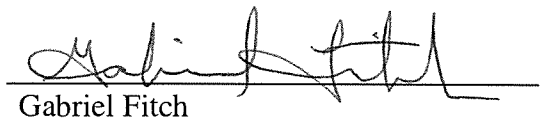
Thirdly, the present invention is now directed to PCB routing. It is well known to skilled workers in the art that channel routing, as forms the basis of Rostoker, is simply unsuitable for PCB routing. Andreev meanwhile wholly concerns IC routing, which again is a different field to PCB routing. For the avoidance of doubt, as is well known to skilled workers in the art, PCB routing requires geometric (free space) routing, which is not disclosed either by Rostoker or Andreev. Accordingly, neither Andreev or Rostoker, considered alone or in proper combination, teaches a method suitable for PCB routing as recited in claim 1. For at least this reason, claim 1 is patentable over the cited references.

For the reasons recited above, claim 1 is patentable over the cited references. Claims 3, 4 depend from claim 1, which is patentably distinguishable for the aforementioned reasons. In addition, claims 3, 4 include terms and limitations which together further patentably distinguish

these claims over the cited references. Therefore, claims 3, 4 are patentably distinguishable over the cited references.

For the aforementioned reasons, Applicant submits that all of the pending claims are allowable. Therefore, Applicant respectfully request a timely issuance of a Notice of Allowance. If Applicants' counsel can be of assistance, please do not hesitate to call the undersigned at the phone number provided below.

Respectfully submitted,
CHRISTIE, PARKER & HALE, LLP

By 
Gabriel Fitch
Reg. No. 62,905
626/795-9900

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